AMENDMENTS TO THE CLAIMS

Please amend the Claims as follows:

1. (Currently Amended) A method of forming a local interconnect on a semiconductor integrated circuit, the method comprising:

forming a gate stack on a substrate, the gate stack having at least one conductive layer and a source layer positioned on top of the at least one conductive layer and at an uppermost surface of the gate stack, the source layer providing a rich source of transforming atoms;

exhuming a first layer of the gate stack so as to expose a portion of the source layer above at least a portion of the gate stack so as to define a first circuit node;

depositing a refractory material ~~on the integrated circuit~~ so that the refractory material contacts the exposed uppermost portion of the source layer of the gate stack and so that the refractory material is also positioned ~~on another device~~ to contact a second circuit node of the integrated circuit having a rich source of the transforming atoms;

forming a masking layer over the refractory material;

etching the masking layer so as to define an extent of the local interconnect; and

selectively transforming the refractory material underneath the etched masking layer ~~including at~~ and at least adjacent the exposed portion of the source layer and the second circuit node into ~~a~~ low resistance contacts ~~between~~ comprising the refractory material ~~and the source layer~~ such that electrical contact between the refractory metal and the at least one conductive level occurs through the source level and wherein the source layer provides transforming atoms to the portion of the refractory material positioned adjacent the exposed uppermost portion of the source layer~~; and~~

~~performing a selective removal process wherein portions of the refractory material beyond the masking layer are preferentially removed and wherein the transformed refractory material underneath the masking layer is preferentially unresponsive to the selective removal process~~.

2. (Previously Presented) The method of Claim 1, wherein the source layer provides the transforming atoms to the refractory material during transformation of the refractory material

such that the selective removal process reduces undercutting of the low resistance contact at the exposed surface of the source layer.

3. (Original) The method of Claim 1, wherein the transforming of the refractory material comprises transforming the refractory material adjacent the source layer into a silicide contact and wherein the transforming atoms of the source layer comprise silicon atoms to transform the refractory material adjacent the source layer into the low resistance contact.

4. (Original) The method of Claim 3, wherein forming a gate stack comprises:

depositing a plurality of blanket layers over a semiconductor substrate; and

removing material from the plurality of blanket layers so as to define the gate stack.

5. (Original) The method of Claim 4, wherein depositing a plurality of blanket layers over a semiconductor substrate comprises depositing a blanket gate oxide layer over the substrate.

6. (Original) The method of Claim 5, wherein depositing a plurality of blanket layers over a semiconductor substrate further comprises depositing an outwardly conductive blanket layer over the blanket gate oxide layer.

7. (Original) The method of Claim 6, wherein depositing an outwardly conductive blanket layer comprises depositing a first blanket polysilicon layer.

8. (Original) The method of Claim 7, wherein depositing a plurality of blanket layers over a semiconductor substrate further comprises depositing a laterally conductive blanket layer over the outwardly conductive blanket layer.

9. (Original) The method of Claim 8, wherein depositing a laterally conductive blanket layer comprises depositing a blanket layer of tungsten silicide.

10. (Original) The method of Claim 9, wherein depositing a plurality of blanket layers over a semiconductor substrate further comprises depositing a blanket source layer over the blanket conducting layer.

11. (Original) The method of Claim 10, wherein depositing a blanket source layer over the blanket conducting layer comprises depositing a second blanket polysilicon layer.

12. (Original) The method of Claim 11, wherein depositing a second blanket polysilicon layer comprises depositing a second blanket polysilicon layer having a thickness between 100 Angstroms and 1000 Angstroms.

13. (Cancelled)

14. (Original) The method of Claim 1, wherein exhuming a first layer of the gate stack comprises removing a portion of a cap insulating layer.

15. (Currently Amended) The method of Claim ~~2~~ 1, wherein depositing refractory material ~~on the integrated circuit~~ comprises depositing a blanket layer of titanium.

16. (Original) The method of Claim 15, wherein depositing a blanket layer of titanium comprises depositing a blanket layer of titanium having a thickness between 100 Angstroms and 500 Angstroms.

17. (Previously Presented) The method of Claim 1, wherein transforming the refractory material comprises annealing the refractory material in a nitrogen containing ambient.

18. (Original) The method of Claim 17, wherein annealing the refractory material comprises exposing the refractory material to a rapid thermal processing environment having an N2/NH3 ambient so as to increase the temperature of the refractory material to a value between 600 degrees Celsius and 750 degrees Celsius for a period of time between 10 seconds and 60 seconds.

19. (Cancelled)

20. (Currently Amended) A method of forming a local interconnect on a semiconductor integrated circuit, the method comprising:

forming a gate stack having at least one conductive layer and a source layer of polysilicon positioned on top of the at least one conductive layer, the source layer of polysilicon providing a rich source of silicon atoms;

exhuming a first layer of the gate stack so as to expose a portion of the source layer above at least a portion of the gate stack so as to define a first circuit node of the integrated circuit;

depositing a refractory material on the integrated circuit so that a portion of the refractory material contacts the exposed portion of the source layer of the gate stack and

so that the refractory material is positioned ~~on another device~~ to contact a second circuit node also providing a rich source of the silicon atoms of the integrated circuit;

forming a masking layer over the refractory material;

etching the masking layer so as to define an extent of the local interconnect defined underneath the masking layer and with portions of the refractory material not underneath the masking layer comprising excess refractory material;

preferentially transforming at least ~~the~~ portions of the refractory material underneath the masking layer ~~including~~ and adjacent the exposed portion of the source layer or adjacent the second circuit node into ~~a~~ conductive silicide contacts such that electrical contact between the refractory ~~metal~~ material and the at least one conductive layer occurs through the source layer wherein the source layer provides silicon atoms to the portion of the refractory material positioned adjacent the exposed portion of the source layer so as to form the respective silicide contact~~; and~~

~~selectively removing the excess refractory material such that the conductive silicide contact is substantially preserved wherein the source layer provides sufficient silicon atoms to the transformed refractory material during transformation of the refractory material to reduce undercutting of the conductive silicide contact at the exposed surface of the source layer~~.

21. (Original) The method of Claim 20, wherein forming a gate stack having at least one conductive layer and a source layer of polysilicon positioned on top of the at least one conductive layer comprises forming a gate stack with a refractory silicide layer immediately underneath a source layer of polysilicon.

22. (Original) The method of Claim 21, wherein forming a gate stack with a refractory silicide layer immediately underneath a source layer of polysilicon comprises forming a gate stack with a tungsten silicide layer immediately underneath a source layer of polysilicon.

23. (Currently Amended) The method of Claim 20, wherein depositing refractory material ~~on the integrated circuit~~ comprises depositing a blanket layer of refractory material comprised of titanium.

24. (Previously Presented) The method of Claim 23, wherein preferentially transforming the refractory material comprises annealing the refractory material in a nitrogen containing ambient.

25. (Previously Presented) The method of Claim 24, wherein selectively removing the excess refractory material comprises

etching the exposed refractory material after annealing the refractory material with etchant which is selective for nitrides and substantially less reactive with silicides.

26. (Previously Presented) The method of Claim 1, wherein the selective removal process comprises a wet etch process selective for nitrides and not for silicides.

Please add the following new Claims:

27. (New) The method of Claim 1, further comprising performing a selective removal process wherein portions of the refractory material beyond the masking layer are preferentially removed and wherein the transformed refractory material underneath the masking layer is preferentially unresponsive to the selective removal process.

28. (New) The method of Claim 1, wherein the masking layer is also a rich source of the transforming atoms and wherein the transforming of the refractory material occurs to substantially all of the refractory material underneath the etched masking layer.